IN THE SPECIFICATION:

Please amend paragraph **[0003]** as follows:

[0003] Background of Related Art: Conventionally, spin-on processes have been used to apply substantially planar layers of material to the surfaces of semiconductor device structures being fabricated upon a wafer of semiconductor material (e.g., a silicon, gallium arsenide, or indium phosphide wafer) or other semiconductor substrate (e.g., a silicon on insulator (SOI), silicon on glass ~~(SOG),silicon~~ (SOG), silicon on ceramic (SOC), silicon on sapphire (SOS), or other similar substrate). Consequently, while the portions of a spun-on layer of material over substantially horizontal structures may be substantially planar, the layer of material may not substantially fill or conform to the numerous, minute recesses formed in the semiconductor device structure.

Please amend paragraph **[0011]** as follows:

[0011] In one embodiment of the present invention, the semiconductor device structure includes a stacked capacitor structure with a layer of electrically insulative material, or insulator layer, and at least one container recessed or formed in the insulator layer. The insulator layer includes a substantially planar surface, which is referred to herein as the exposed surface of the insulator layer. A layer of electrically conductive material covers the surface of the insulator layer and lines the at least one container. By way of example, the electrically conductive material may be conductively doped hemispherical grain (HSG) silicon. As the stacked capacitor structure would electrically short if the conductive material remained on the surface of the insulator layer between adjacent containers, for the stacked capacitor to function properly, the conductive material must be removed from the surface of the insulator layer prior to completing fabrication of the stacked capacitor but remain within the containers. Thus, this embodiment of the semiconductor device structure includes a substantially planar surface with a ~~non-chemical-mechanical~~ nonchemical-mechanical planarized quantity of mask material substantially filling the at least one container. While the mask material may cover regions of the layer of conductive material overlying the surface of the insulator layer, it is preferred that these regions are

substantially uncovered by mask material. If mask material does overlie these regions of the layer of conductive material, the thickness of the mask material overlying these regions is less than the depth of the at least one container. Preferably, the thickness of the mask material over these regions of the layer of conductive material is less than about half the depth of the at least one container.

Please amend paragraph **[0016]** as follows:

[0016] By way of example, the semiconductor device structure may be a shallow trench isolation structure including a semiconductor substrate with a substantially planar surface and trenches recessed, or formed, in the semiconductor substrate. The trenches are filled with a first, electrically insulative material, which is preferably a low dielectric constant, or ~~"low-k",~~ "low-k," material, such as a high density plasma (HDP) silicon oxide, or HDP oxide. HDP oxide or another insulative material may be disposed into the trenches by way of known processes, such as chemical vapor deposition (CVD) processes. As the processes that are used to fill the shallow trenches with the first, insulative material are typically blanket deposition processes, the insulative material may also cover the surface of the semiconductor substrate. The surface of a layer of the first, insulative material blanket deposited over a semiconductor substrate with trenches formed therein is nonplanar.

Please amend paragraph **[0042]** as follows:

[0042] Referring now to FIG. 3, once a mask layer 18 with a substantially planar surface 19 (see FIG. 2) is formed, the portions of mask layer 18 and of hemispherical grain silicon layer 16 that are located above a plane of surface 12 are removed from stacked capacitor structure 10. In order to reduce or eliminate the creation of potentially contaminating debris and of surface defects that may be caused by mechanical planarization processes, layers 18 and 16 are removed by known chemical processes, such as dry etch processes or wet etch, or wet dip, processes. For example, mask layer 18 may be selectively removed by use of a known resist strip, then layer 16 removed from surface 12 with a wet etchant that removes silicon with

selectivity over the portions of mask layer 18 remaining in containers 14 and over an underlying dielectric layer 15. As another example, layers 18 and 16 may be substantially concurrently removed with an etchant or combination of etchants that will remove mask layer 18 and hemispherical grain silicon layer 16 at substantially the same rates. Mask material remaining in containers 14 may then be removed by known processes, such as the use of known wet or dry strip materials (e.g., an ammonium hydroxide (NH_4OH) dry strip known in the art as a "piranha" strip when the mask material is ARCH 895 or a similar photoresist). This process provides a stacked capacitor structure 10 with conductively doped hemispherical grain silicon 16-lined containers 14 recessed in a substantially ~~defect and~~ defect- and contaminant-free surface 12 of structure 10 and dielectric layer 15, as shown in FIG. 4. Stacked capacitor structure 10 shown in FIG. 4 may then be processed as known in the art to fabricate a finished stacked capacitor.

Please amend paragraph **[0043]** as follows:

[0043] Turning now to FIGs. 5 and 6, another embodiment of a semiconductor device structure, in this instance a shallow trench isolation structure 20, incorporating teachings of the present invention is illustrated. FIG. 5 depicts a shallow trench isolation structure 20 that includes a semiconductor substrate 21 formed from silicon, gallium arsenide, indium phosphide, or another suitable semiconductor material, and which may be in the form of a wafer or another substrate, such as a silicon-on-glass, silicon-on-sapphire, silicon-on-ceramic, or other ~~silicon-on-insulator~~ silicon-on-insulator type substrate. Semiconductor substrate 21 includes a surface 22 with one or more trenches 24 recessed, or formed, therein. Trenches 24 may be formed in semiconductor substrate 21 by known techniques, such as mask and etch processes. Shallow trench isolation structure 20 also includes a mask layer 28 with a substantially planar surface 29. Mask layer 28 substantially fills trenches 24 and may also cover surface 22 of semiconductor substrate 21. As shown in FIG. 5, the thickness T′ of portions of mask layer 28 overlying surface 22 is less than the depth D′ of trenches 24. Preferably, thickness T′ is less than about half of depth D′. Alternatively, surface 22 may remain substantially uncovered by mask layer 28. Mask layer 28 may be formed from a photoresist or other polymer by processes the same as or

similar to those described previously herein with reference to the fabrication of mask layer 18 illustrated in FIG. 2.

Please amend paragraph **[0050]** as follows:

[0050] Alternatively, once a substantially planar surface 31 has been formed over shallow trench isolation structure 30, as shown in FIG. 9, stress buffer layer 38′ and the portions of insulator layer 36 located above the plane of surface 22 may be substantially concurrently removed from above shallow trench isolation structure 30 by use of one or more dry or wet etchants that remove the materials of ~~layers 38~~ layers 38′ and 36 at substantially the same rates, as known in the art, or by known chemical-mechanical planarization processes to provide the finished shallow trench isolation structure 30 illustrated in FIG. 11.

Please amend paragraph **[0052]** as follows:

[0052] FIGs. 12-16 illustrate yet another embodiment of a semiconductor device structure 40 that incorporates teachings of the present invention. With reference to FIGs. 12 and 13, semiconductor device structure 40 includes dual damascene trenches 44 formed in a surface 42 of an insulator layer 41 thereof. As shown, one or more of trenches 44 may expose a conductively doped region 23 of a semiconductor substrate 21 of semiconductor device structure 40, which conductively doped region 23 is continuous with a surface 22 of semiconductor substrate 21. A conductive layer 46 overlies surface 42 and substantially fills trenches 44. Conductive layer 46 has a nonplanar upper surface 47 that includes valleys 54 located substantially over trenches 44 and peaks 52 located substantially over surface 42. Insulator layer 41, trenches 44, and conductive layer 46, as well as other structures of semiconductor device structure 40 underlying insulator layer 41 and trenches 44 are each fabricated by known processes, such as those disclosed in U.S. Patent 5,980,657 to Farrar et al. issued on November 9, 1999, the disclosure of which is hereby incorporated in its entirety by this reference.

Please amend paragraph **[0054]** as follows:

[0054] Once a substantially planar surface is formed over semiconductor device structure 40, such as that formed at least partially by surface 49 of stress buffer layer 48 and as illustrated in FIG. 12, stress buffer layer 48 and portions of conductive layer 46 located above the plane of surface 42 may be substantially concurrently removed. For example, layers 48 and 46 may be substantially concurrently removed with an etchant or combination of etchants that will remove stress buffer layer 48 and ~~insulator~~ conductive layer 46 at substantially the same rates to provide the finished semiconductor device structure 40 illustrated in FIG. 16. Either wet etchants or dry etchants may be used. Preferably, the use of etchants eliminates the formation of imperfections or defects in surface 42 of insulator layer 41, as well as the possible introduction of contaminants or other debris thereon. Alternatively, known chemical-mechanical planarization processes may be used to substantially concurrently remove stress buffer layer 48 and portions of conductive layer 46 above surface 42, also providing a finished semiconductor device structure 40 such as that illustrated in FIG. 16. As stress buffer layer 48 provides a substantially planar surface over ~~shallow trench isolation~~ semiconductor device structure 40, the likelihood that material of conductive layer 46 will be broken off during the chemical-mechanical planarization process is reduced, thereby reducing the formation of imperfections or defects in surface 42, as well as the creation of contaminants or other debris, which may occur during chemical-mechanical planarization of a nonplanar surface.

Please amend paragraph **[0055]** as follows:

[0055] As illustrated in FIG. 13, stress buffer layer 48′ may not provide semiconductor device structure 40 with a substantially planar surface. Rather, peaks 52 of conductive layer 46 protrude above surface 49′ of stress buffer layer 48′. In order to provide a substantially planar surface over semiconductor device structure 40, the portions of peaks 52 that protrude above the plane of surface 49′ may be selectively removed, such as by use of selective wet or dry etch processes. The material of peaks 52 that protrudes above the plane of surface 49′ is removed at least until a substantially planar surface 51 is formed over semiconductor device structure 40, as depicted in ~~FIG.14.~~ FIG. 14.